A Step-up 25-level Inverter Topology for Photovoltaic Systems

Fatemeh Esmaeili, Hamid Reza Koofigar, Frede Blaabjerg, *Fellow*, *IEEE*

***Abstract*—Integration of renewable energy sources into power systems requires efficient multilevel inverters, capable of producing high-quality output voltage with low total harmonic distortion (THD). Conventional multilevel inverters often suffer from high component count, high switching stress, low voltage gain, and increased cost, limiting their practical application. This paper introduces a high-gain novel topology for multilevel inverters with reduced number of total components per level count, low voltage stress on power conductive devices, and minimizing a cost function, which depends on the number of components, standing voltage on switches and diodes, output voltage levels, and gain. The designed topology, which can be applied in photovoltaic (PV) systems, utilizes only one direct current (DC) input supply and a modular structure with the ability of capacitor's voltage self-balancing. The high gain property and low THD of the proposed topology are two advantages that provide sine output waveform, with no need to a high DC input voltage source. Moreover, generalized topology, consisting of cascaded basic units, has been proposed. A comprehensive method has been proposed to determining the values of DC supplies in this configuration, aiming to minimize redundant switching modes and maximize the voltage levels count. The comparison with some other multilevel inverters confirms the desired performance of the basic version given inverter. A prototype has been also implemented and the experimental results have been obtained to verify the advantages of the proposed 25-level topology.**

***Index Terms*—Multilevel inverter, Lowering voltage stress, High gain, Low total harmonic distortion (THD).**

I. INTRODUCTION

THE integration of renewable energy into power systems is an inevitable trend for the future, which has experienced significant growth over the past decade [1]-[2]. Multilevel converters play a main role in extracting power from renewable energy sources and delivering an output sine voltage with low total harmonic distortion (THD) to the grid. Some other various applications of such inverters include electric vehicle drives, motor drives, high voltage direct current (DC), marine propulsion systems, and flexible alternating current (AC) transmission systems [3]-[5]. Multilevel-inverters generate a stepped voltage waveform that closely approximates a pure sinusoidal signal with lower THD compared to a two-level/three-level voltage waveform [6]. Simple and modular structure, smaller output filter, lower dv/dt (sudden changes of voltage v with respect to time t) at the output voltage, reduced switching components' blocking voltage, expandability, and suitability for medium/high voltage/power utilities are some of the general benefits of the multilevel inverters [7]-[8]. In medium-voltage renewable energy applications, switched-capacitor-based multilevel inverter topologies have recently attracted considerable attention due to their inherent voltage boosting capability and reduced requirement for multiple isolated DC sources. However, despite these advantages, medium-voltage operation introduces challenges such as increased capacitor voltage stress, voltage balancing issues, and higher component rating requirements, as reported in recent studies on medium-voltage inverter technologies [9].

Multilevel inverters may be classified into two categories, multilevel inverters with multiple DC supply-based and multilevel inverters with single DC supply [10]. A five-level topology is presented in [11], which consists of 6 switches and two input DC sources. However, due to the low power quality of this structure, the need for a filter on the load side becomes essential. In order to increase power quality, a 21-level topology is presented by utilizing three DC sources, whereas the number of required switches is ten [12]. Moreover, in [13], a 31-level inverter is presented, featuring 4 DC input sources and 12 power switches. This design achieves an output voltage waveform that closely approximates a sine wave. Using ten power switches with four capacitors and four DC supplies, a 35-level topology is given in [14]. High number of levels per switch counts is one of the main benefits of the presented structure. A 25-level converter with low voltage/current THD is also constructed, which includes 2 DC supplies, 4 capacitors, and 10 switches/diodes [15]. The high number of steps per device counts has been the major merit of this configuration. Also, several advanced multilevel inverter structures have been introduced, such as pencil-shaped [16], diamond-shaped [17], cross-switched neutral point clamped (NPC) [18], asymmetric T-type [19], and cross-switched T-type topologies [20], aiming to reduce

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component count. In particular, the pencil-shaped multilevel inverter reported in [16] employs a compact structure with directional and bidirectional switches to generate positive and negative voltage levels. Although this topology demonstrates high efficiency and reduced total standing voltage, it relies on multiple DC sources and bidirectional switches, which increase control complexity and limit its suitability for single-source photovoltaic systems. Moreover, the modular extension of pencil-shaped multilevel inverter requires careful coordination of multiple DC supplies. Similarly, the diamond-shaped multilevel inverter proposed in [17] operates in switched-capacitor and asymmetric DC-source modes to generate multiple voltage levels with voltage boosting capability. Despite its reduced total standing voltage and self-balancing capacitors, the diamond-shaped topology exhibits limited scalability in switched-capacitor mode and requires additional DC sources to achieve higher voltage levels in asymmetric operation, which increases system cost and complexity. Cross-switched T-type topologies have been introduced to generate negative voltage levels inherently and to reduce harmonic distortion by increasing the number of voltage levels [20]. However, cross-switched T-type inverters require multiple bidirectional switches, diodes, and DC sources, leading to increased total standing voltage, complex switching sequences, and higher conduction losses, particularly when extended to asymmetric configurations for higher voltage levels. Such high-level inverters are particularly advantageous in applications like renewable energy [21], electric vehicles [22], and high-power drives, where efficiency and performance are critical. On the other hand, the large number of input sources results in a high total cost. The requirement of more than one input DC supply in multilevel-inverters is an issue to be solved for applications with a single DC supply [23]. The structures with only one DC source reduce the overall volume and cost of the topology. On the other hand, the capability to boost voltage becomes crucial, when designing inverters for renewable energy systems. In other words, the output voltage from photovoltaic panels or fuel cells, which is relatively low, must be increased to a higher standard DC-bus voltage for grid-tied applications. Hence, several high-gain single DC-source multilevel inverters have been proposed in the literature. A nine-level inverter with boosting capability has been reported in [24], by using ten switches, and two capacitors to get a gain of two. While, the topology proposed in [25] is a nine-level inverter with boosting capability of four. With the same number of output voltage levels, an inverter with a higher gain requires less input voltage value to produce the same output voltage. An introduced 5-level inverter in [26] consists of two capacitors, seven switches, and one DC supply. The configuration is unable to combine all capacitor voltages with the input DC supply, which restricts its boosting capability and the production of output voltage levels. Also, the THD of output voltage in [26] is high. Charging the capacitors in a self-balancing manner, a 13-level structure is discussed in [27], eliminating the need for complex modulations. The output voltage gain of this topology is six with thirteen switches, three diodes, three capacitors, and one DC supply. To improve the voltage gain and reduce the THD, a new 17-level high-gain inverter topology with a reduced number of components is introduced in [28]. This design features low THD in both output voltage and load current and achieves a voltage gain of 8. In brief, some main drawbacks of the existing high-gain single DC source multilevel inverters are as follows: (1) needing numerous devices to produce an increased step output voltage waveform; (2) low enhancement capability of the configurations; (3) low power quality of output voltage waveform, due to lower number of levels; (4) high total standing voltage of the structures. Hence, the current research scope is on developing a high-gain topology that requires lower number of components, provides higher boosting factor, and lower total blocking voltage (TBV).

Taking into account the aforementioned issues, a single-phase 25-level inverter has been proposed, having the following features:

1) A 25-level inverter topology with only one DC source, 14 switches, one diode, and 4 capacitors.

2) Low number of components along with low average of voltage stress on power switches and diodes.

3) Low THD of voltage, about 2%, with an output voltage gain of 12.

4) Compared to some similar topologies, minimizing a cost function, which depends on component count, blocking voltage on semiconductors, number of output voltage levels, and gain.

Following this introduction, the proposed converter is detailed, and the operating modes are delineated. Then, the generalized proposed topology is described. Subsequently, comparative analyses between the proposed multilevel inverter and some similar topologies are conducted. Finally, simulation and experimental results from a prototype are presented and discussed to demonstrate the practicality of the proposed topology.

II. Proposed 25-level Inverter Structure

A. Circuit Structure

The suggested single-phase 25-level inverter, schematically illustrated in Fig. 1, comprises a capacitor switching module (CSM) and an H-bridge module (HBM). The HBM transfers the positive voltage generated by the CSM into the load terminals and can also generate negative polarity. In the given configuration, only one input DC source (with the magnitude of V_{dc}) is used, which may be photovoltaic panels, fuel cell, or battery. For $1V_{dc}$ input supply, the given topology can generate a 25-step AC output voltage, due to its voltage-boosting capability. To this end, one power source, four capacitors, one diode, and fourteen switches are required.

B. Capacitors' Balancing Analysis

The capacitor C_1 can be charged by the input supply (V_{dc}), through the charging switching components (i.e., S_2 and D_1), depending on different switching modes of HBM. For charging capacitor C_2, S_3 and S_5 need to be turned on, the

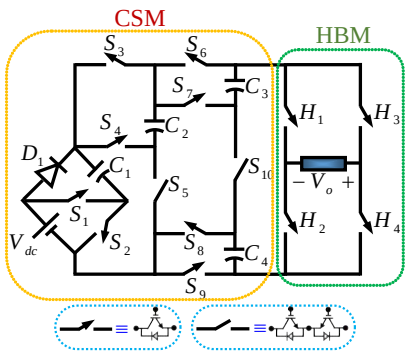


Fig. 1. Circuit diagram of the suggested 25-level inverter.

supply needs to be input, and capacitor C_1 should be in series (switch S_1 needs to be turned on). In this mode, C_2 is charged up to $2V_{dc}$ and switch S_4 is inactive during this mode. Capacitors C_3 and C_4 are charged up to $4V_{dc}$, when the input supply, capacitor C_1 and capacitor C_2 are connected in series with each other. In such a way, when switches S_1, S_4, S_6, S_8, and S_{10} are turned on, capacitor C_3 is placed in parallel with the input sources, C_1 and C_2. When switches S_1, S_4, S_7, S_9, and S_{10} are turned on, capacitor C_4 is placed in parallel with the input source, C_1 and C_2. Mathematically, it can be written as

$$\begin{aligned} V_{C1} &= V_{dc} \\ V_{C2} &= V_{dc} + V_{C1} = 2\,V_{dc} \\ V_{C3} &= V_{dc} + V_{C1} + V_{C2} = 4\,V_{dc} \\ V_{C4} &= V_{dc} + V_{C1} + V_{C2} = 4\,V_{dc} \end{aligned} \tag{1}$$

where V_{C1}, V_{C2}, V_{C3}, and V_{C4} represent the voltages of capacitors C_1, C_2, C_3, and C_4, respectively.

C. Analysis of Switches Voltage Stress

The switching modes of the suggested 25-step inverter are summarized in Table I, in which "0" and "1" indicate the switches being in the OFF and ON states, respectively.

TABLE I
SWITCHING MODES, AND OUTPUT VOLTAGE OF THE SUGGESTED INVERTER IN FIG. 1

Output	Remark	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	D	H_1	H_2	H_3	H_4
$12V_{dc}$	$V_{dc}+V_{C1}+V_{C2}+V_{C3}+V_{C4}$	1	0	0	1	0	0	1	1	0	0	0	0	1	1	0
$11V_{dc}$	$V_{dc}+V_{C2}+V_{C3}+V_{C4}$	0	1	0	1	0	0	1	1	0	0	1	0	1	1	0
$10V_{dc}$	$V_{dc}+V_{C1}+V_{C3}+V_{C4}$	1	0	1	0	1	0	1	1	0	0	0	0	1	1	0
$9V_{dc}$	$V_{dc}+V_{C3}+V_{C4}$	0	1	1	0	0	0	1	1	0	0	1	0	1	1	0
$8V_{dc}$	$V_{dc}+V_{C1}+V_{C2}+V_{C4}$	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0
$7V_{dc}$	$V_{dc}+V_{C2}+V_{C4}$	0	1	0	1	0	1	0	1	0	0	1	0	1	1	0
$6V_{dc}$	$V_{dc}+V_{C1}+V_{C4}$	1	0	1	0	1	1	0	1	0	0	0	0	1	1	0
$5V_{dc}$	$V_{dc}+V_{C4}$	0	1	1	0	0	1	0	1	0	0	1	0	1	1	0
$4V_{dc}$	$V_{dc}+V_{C1}+V_{C2}$	1	0	0	1	0	1	0	0	1	0	0	0	1	1	0
$3V_{dc}$	$V_{dc}+V_{C2}$	0	1	0	1	0	1	0	0	1	0	1	0	1	1	0
$2V_{dc}$	$V_{dc}+V_{C1}$	1	0	1	0	1	1	0	0	1	0	0	0	1	1	0
V_{dc}	V_{dc}	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1
$-V_{dc}$	$-V_{dc}$	0	1	1	0	0	1	0	0	1	0	1	1	0	0	1
$-2V_{dc}$	$-(V_{dc}+V_{C1})$	1	0	1	0	1	1	0	0	1	0	0	1	0	0	1
$-3V_{dc}$	$-(V_{dc}+V_{C2})$	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1
$-4V_{dc}$	$-(V_{dc}+V_{C1}+V_{C2})$	1	0	0	1	0	1	0	0	1	0	0	1	0	0	1
$-5V_{dc}$	$-(V_{dc}+V_{C3})$	0	1	1	0	0	0	1	0	1	0	1	1	0	0	1
$-6V_{dc}$	$-(V_{dc}+V_{C1}+V_{C3})$	1	0	1	0	1	0	1	0	1	0	0	1	0	0	1
$-7V_{dc}$	$-(V_{dc}+V_{C2}+V_{C3})$	0	1	0	1	0	0	1	0	1	0	1	1	0	0	1
$-8V_{dc}$	$-(V_{dc}+V_{C1}+V_{C2}+V_{C3})$	1	0	0	1	0	0	1	0	1	1	0	1	0	0	1
$-9V_{dc}$	$-(V_{dc}+V_{C3}+V_{C4})$	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1
$-10V_{dc}$	$-(V_{dc}+V_{C1}+V_{C3}+V_{C4})$	1	0	1	0	1	0	1	1	0	0	0	1	0	0	1
$-11V_{dc}$	$-(V_{dc}+V_{C2}+V_{C3}+V_{C4})$	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1
$-12V_{dc}$	$-(V_{dc}+V_{C1}+V_{C2}+V_{C3}+V_{C4})$	1	0	0	1	0	0	1	1	0	0	0	1	0	0	1

The switching modes of the given inverter are depicted in Fig. 2. It illustrates that the suggested topology can generate 25 voltage levels with the peak output voltage of $V_{o,max} = 12V_{dc}$. The gain, defined as the ratio of the peak output voltage to the sum of the magnitudes of the DC input sources, is 12, which is analytically expressed as:

$$\text{Gain} = \frac{V_{o,max}}{V_{dc}} = 12 \tag{2}$$

The blocking voltage (BV) and normalized BV (NBV) on semiconductors of the given 25-level converter are shown in Table II. The NBV is defined as NBV = (BV/$V_{o,max}$), where $V_{o,max}$= $12V_{dc}$. Except for switches H_1-H_4 and S_{10} that suffer from the $V_{o,max}$ and $0.5V_{o,max}$ blocking voltage, the remaining switches withstand equal to or less than 33% of $V_{o,max}$. Also, the blocking voltage of the diode D_1 is about 8% of $V_{o,max}$. The low BVs result in smaller switch sizes, reduced losses, and lower costs.

TABLE II
BLOCKING VOLTAGE AND NORMALIZED BLOCKING VOLTAGE ON SEMICONDUCTORS OF THE PROPOSED 25-LEVEL INVERTER TOPOLOGY

Semiconductor	BV	NBV/%	Semiconductor	BV	NBV/%
S_1	V_{dc}	8.33	S_9	$4V_{dc}$	33.33
S_2	V_{dc}	8.33	S_{10}	$6V_{dc}$	50
S_3	$2V_{dc}$	16.66	H_1	$12V_{dc}$	100
S_4	$2V_{dc}$	16.66	H_2	$12V_{dc}$	100
S_5	$2V_{dc}$	16.66	H_3	$12V_{dc}$	100
S_6	$4V_{dc}$	33.33	H_4	$12V_{dc}$	100
S_7	$4V_{dc}$	33.33	D_1	V_{dc}	8.33
S_8	$4V_{dc}$	33.33			

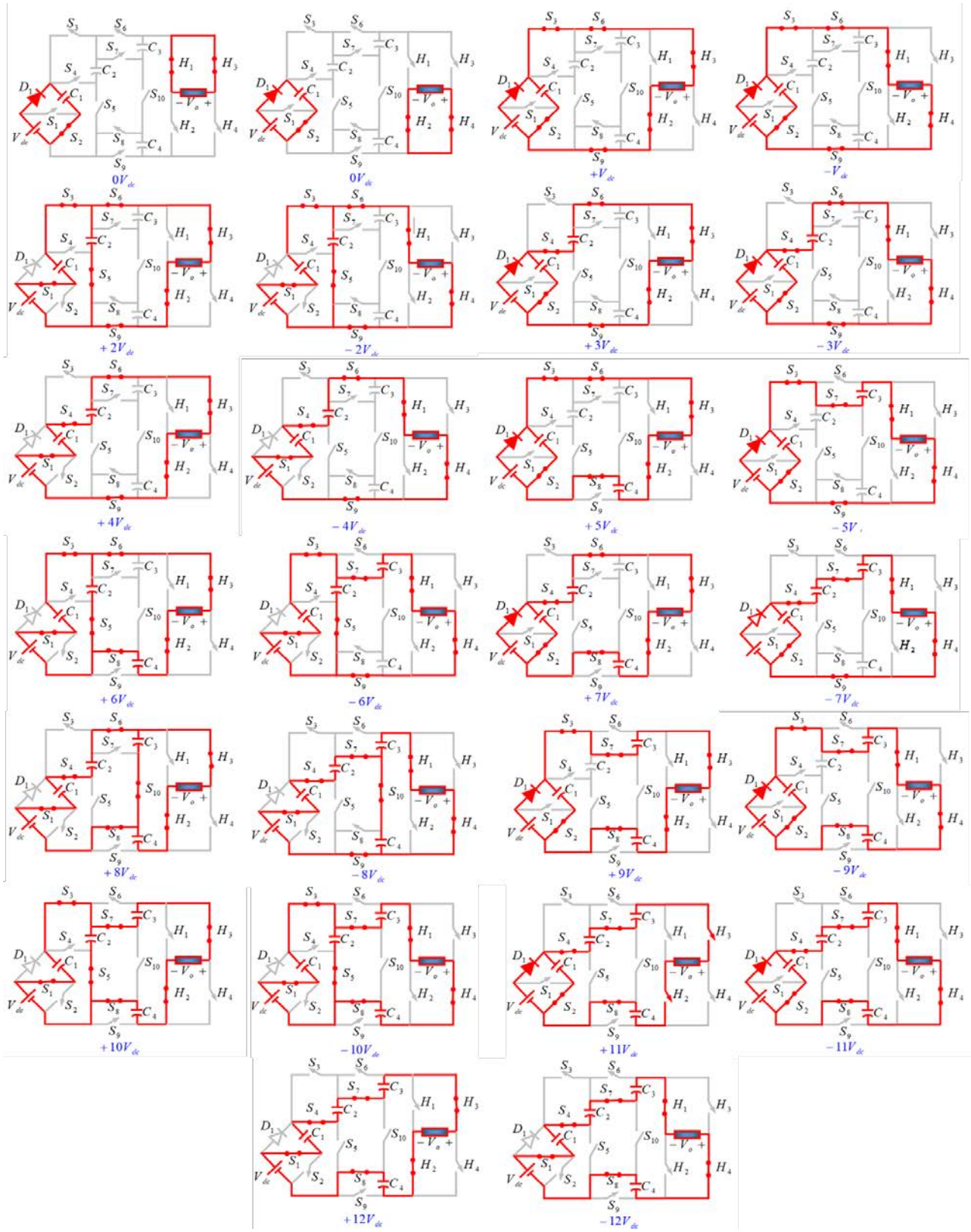


Fig. 2. The different operational modes of output voltage levels of the proposed converter.

Average of BV (ABV) and average of NBV (ANBV) on the semiconductors of 25-level inverter can be obtained by:

$$\mathrm{ABV} = \frac{\sum \mathrm{BV}_{\mathrm{S,H}}}{N_{\mathrm{switch\&diode}}} = 5.26V_{\mathrm{dc}} \tag{3}$$

$$\mathrm{ANBV} = \frac{\sum \mathrm{BV}_{\mathrm{S,H}}}{N_{\mathrm{switch\&diode}} \times V_{\mathrm{o,max}}} \times 100\% = 43\% \tag{4}$$

D. Modulation Method

This study employs the nearest-level method for producing

the switching pulses [29]. In such technique, a 50 Hz sinusoidal reference waveform with magnitude of A_{ref} is contrasted with predictable voltage levels (V_{ref} = 12sin(100πt)). The closest voltage level to the reference signal is generated at the output continuously, as depicted in Fig. 3(a), along with charging/discharging mode of capacitors.

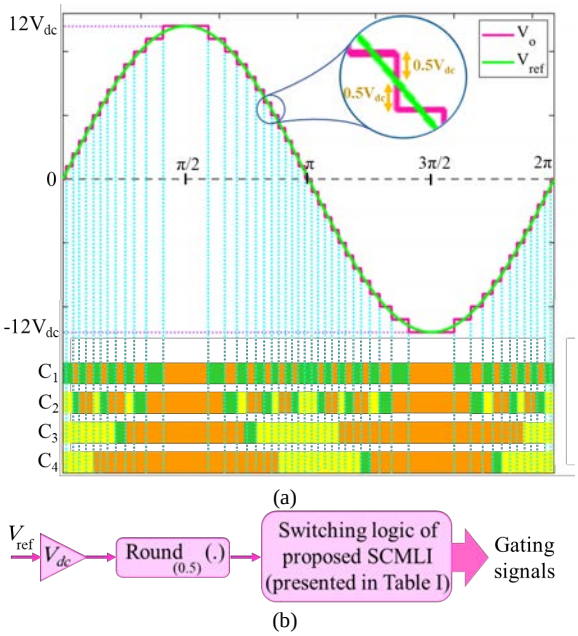


Fig. 3. Nearest-level technique. (a) Modulation method of the suggested structure, along with charging (■), discharging (■), and no charging (■) of the capacitors C_1-C_4. (b) Control diagram flowchart.

This method minimizes the switching losses by ensuring switches activate only when the reference voltage closely aligns with a predefined level, resulting in a low switching frequency, improved efficiency, and reduced thermal stress on the semiconductors. Additionally, in multi-level topologies, the mentioned technique enhances the output waveform quality by generating higher resolution voltage steps without relying on complex modulation algorithms, and thereby contributing to better performance and stability.

In the literature, various modulation strategies have been applied for multilevel converters, particularly in open-loop operation. Space vector modulation (SVM) and selective harmonic elimination (SHE) techniques provide high-quality output voltage with low THD, but their implementation is relatively complex and computationally demanding, which limits their practicality for real-time open-loop operation [30]-[31]. Pulse width modulation (PWM) is straightforward and suitable for high switching frequency applications; however, it results in increased switching losses and thermal stress on the semiconductors. In contrast, the nearest level or fundamental frequency switching method is simple, easily implemented, and operates at low switching frequency, resulting in low switching losses, reduced thermal stress, and effective staircase voltage generation in open-loop multilevel inverters. Considering these trade-offs, the nearest-level method has been adopted for the proposed 25-level inverter. This approach not only maintains efficient capacitor voltage balancing and low switching losses but also produces a staircase output voltage with acceptable quality, making it well-suited for practical open-loop photovoltaic (PV) applications. The implementation steps of the nearest-level algorithm are illustrated in Fig. 3(b) as a flowchart, enabling reproducibility of the method.

E. Fault-tolerant (FT) Operation

FT operation, which refers to the ability of converters to maintain stable performance during various failures, is evaluated for the proposed structure in the event of any switch failures. Table III summarizes the redundant modes of the suggested topology during the open-circuit failure of each switch. If any of the switches S_1, S_2, S_4, S_5, S_7, S_8, S_{10} encounter a failure, power conversion continues, with reduced levels (from 25-level to 13-level, or 9-level) in the voltage output, which can give a good FT capability of the proposed structure.

TABLE III
REDUNDANT MODES OF THE SUGGESTED TOPOLOGY DURING THE OPEN-CIRCUIT FAILURE OF EACH SWITCH

Failed-switch	Available states	Operation level
S_1, S_2, S_4, S_5, S_8, S_7	0, ±V_{dc}, ±2V_{dc}, ±3V_{dc}, ±4V_{dc}, ±5V_{dc}, ±6V_{dc}	13-level
S_{10}	0, ±V_{dc}, ±2V_{dc}, ±3V_{dc}, ±4V_{dc}	9-level

III. PROPOSED GENERALIZED MULTILEVEL INVERTER

A. Topology

The proposed generalized topology may be achieved by cascading the basic modules, as depicted in Fig. 4. This topology includes n input DC sources, 14n switches, n diodes, 4n capacitors, and 14n gate drivers, as indicated in (5). Specifically, 12n unidirectional switches and 2n bidirectional switches are needed. The total count of the required components for this generalized topology is N_{TC} = 34n, where n represents the number of cascaded units.

$$N_{DC} = N_{diode} = n, N_{switch} = N_{driver} = 14n, \\ N_{capacitor} = 4n, N_{IGBT} = 16n, N_{TC} = 34n \quad (5)$$

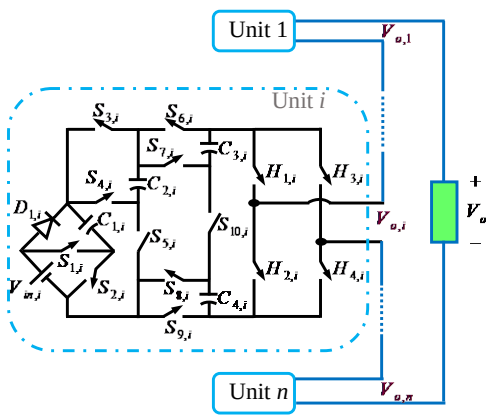


Fig. 4. Circuit diagram of the proposed generalized inverter.

B. Determining the Appropriate Magnitude of the DC Sources

The magnitude of the DC sources directly influences the levels in multilevel inverters. This section introduces an algorithm for determining the values of DC sources within the proposed generalized architecture, with the goal to reduce redundant states and enhancing the number of levels. In this algorithm, $V_{\text{in},i}$ denotes the input DC source of the i^{th} cascaded unit, with its magnitude determined by adding V_{dc} to the maximum output voltage produced by the preceding sources, as shown in (6).

$$\begin{aligned} V_{in.1} &= V_{\text{dc}} \\ V_{\text{in},i} &= \sum_{j=1}^{i-1}(V_{\text{o,max}_j}) + V_{\text{dc}},\ i = 2,\ldots,n \end{aligned} \tag{6}$$

By simplifying (6), using a recursive relation series, the value of the input DC supplies for the i^{th} unit may be determined as:

$$V_{\text{in},i} = 13^{i-1} \tag{7}$$

The peak output voltage and the number of steps in the given configuration with n cascaded modules can be calculated as:

$$V_{\text{o,max}} = 13^n - 1 \tag{8}$$

$$N_{\text{level}} = 2 \times 13^n - 1 \tag{9}$$

The Gain of the proposed generalized topology with n cascaded units, using (7)-(8), and recursive relation series, may be calculated as:

$$\text{Gain} = \frac{V_{\text{o,max}}}{\sum_{i=1}^{n} V_{\text{in},i}} = 12 \tag{10}$$

C. Calculations of Voltage Stress

The blocking voltage on the semiconductor devices of the proposed cascaded converter is examined, and the following equation illustrates the relation for the BV on the switches and diode of the i^{th} unit in the proposed generalized structure.

$$\begin{aligned} &\text{BV}_{S_{1,i}} = \text{BV}_{S_{2,i}} = \text{BV}_{D_{1,i}} = \text{V}_{\text{in},i} \\ &\text{BV}_{S_{3,i}} = \text{BV}_{S_{4,i}} = \text{BV}_{S_{5,i}} = 2V_{\text{in},i} \\ &\text{BV}_{S_{6,i}} = \text{BV}_{S_{7,i}} = \text{BV}_{S_{8,i}} = \text{BV}_{S_{9,i}} = 4V_{\text{in},i} \\ &\text{BV}_{S_{10,i}} = 6V_{\text{in},i} \\ &\text{BV}_{H_{1,i}} = \text{BV}_{H_{2,i}} = \text{BV}_{H_{3,i}} = \text{BV}_{H_{4,i}} = 12V_{\text{in},i} \end{aligned} \tag{11}$$

Thus, by using (11), the TBV on the switches of the i^{th} unit can be calculated as:

$$\text{TBV}_i = \sum \text{BV}_{S_i,H_i,D_i} = 79\,V_{\text{in},i} \tag{12}$$

The TBV for the proposed generalized structure with n cascaded units may be determined by substituting (7) into (12) and summing the TBV for each cascaded unit (TBV_i), as shown in (13):

$$\text{TBV} = \sum \text{TBV}_i = \frac{79}{12}\left(13^n - 1\right) \tag{13}$$

IV. Comparison Study

To highlight the advantages of the given converter, a comparison study is conducted between the proposed circuit and other high-gain multilevel-inverters [24], [29], [32]-[40], across various metrics including the number of DC input supplies (N_{DC}), number of semiconductors ($N_{\text{semiconductor}}$), number of capacitors (N_{C}), number of total components (N_{TC}), Gain, and cost function (CF). The compared structures are summarized in Table IV. The selection of inverter topologies included in the comparative analysis is carried out based on a fair and consistent comparison methodology. Specifically, the compared multilevel inverters are categorized according to the number of output voltage levels and the number of DC sources employed. For lower-voltage levels (e.g., 9-11 levels), only single-DC-source topologies are considered. For medium voltage levels (13-19 levels), single- and two-source multilevel inverters are selected. Finally, for high voltage levels comparable to the proposed inverter (25-level), the comparison is restricted to topologies with similar output voltage levels and comparable DC-source diversity.

TABLE IV
COMPARED TOPOLOGIES' INFORMATION

Parameters	[32]	[33]	[29]	[34]	[35]	[36]	[37]	[38] sym.	[24] sym.	[39] sym.	[40] sym.	Proposed
N_{level}	9	9	11	13	17	17	19	25	25	25	25	25
$N_{\text{semiconductor}}$	9	13	13	18	14	14	22	23	30	54	44	15
N_{DC}	1	1	1	2	1	2	1	3	3	6	4	1
N_{C}	2	2	4	4	3	3	3	6	6	6	8	4
N_{TC}	20	26	27	40	30	30	45	52	69	120	100	34
$\text{TBV}_{\text{pu}} = \text{TBV}/V_{\text{o,max}}$	5	4.5	6.6	5.6	6.5	2.68	2.11	4.67	2.75	4.5	5.33	6.41
$V_{\text{o,max}}$	$2V_{\text{dc}}$	$4V_{\text{dc}}$	$5V_{\text{dc}}$	$6V_{\text{dc}}$	$4V_{\text{dc}}$	$8V_{\text{dc}}$	$9V_{\text{dc}}$	$12V_{\text{dc}}$	$12V_{\text{dc}}$	$12V_{\text{dc}}$	$12V_{\text{dc}}$	$12V_{\text{dc}}$
Gain	2	4	5	3	4	1.6	9	2	2	2	3	12
CF	1.389	0.85	0.611	1.16	0.536	1.2	0.275	1.133	1.435	2.49	1.4	0.134

N_{level}: number of output voltage levels; $N_{\text{semiconductor}}$: number of semiconductors; N_{DC}: number of DC input supplies; N_{C}: number of capacitors; N_{TC}: number of total components; TBV_{pu}: total blocking voltage in per unit; $V_{\text{o,max}}$: maximum output voltage; Gain: boosting factor; CF: cost function

As depicted in Table IV, [34] and [36] need two input DC supplies to generate 13-step and 17-step output, respectively, and [24], [38]-[40] require more than two input supplies to generate 25-level output, unlike the suggested topology that

requires just one input supply. Also, from Fig. 5(a), it is clear that the number of levels per DC source count of the suggested topology is higher than the others. It means that the proposed structure needs fewer DC source counts for the same levels. The given circuit has higher number of steps per total component count, as demonstrated in Fig. 5(b). Therefore, the compared structures need high number of components such as semiconductors (power switches and diodes) in comparison with the proposed topology. The total number of components is defined as N_{DC}+$N_{capacitor}$+N_{switch}+N_{driver}+N_{diode}. The voltage boosting capability is considered a merit for topologies of the newer presented multilevel inverters. In comparison with other topologies, the proposed circuit can step up the output voltage to 12 times. Fig. 5(c) shows that the gain per total components count of the given topology is higher than that of the other topologies. Also, from Fig. 5(d), the proposed structure provides a higher gain with fewer sources compared to other structures. One of the main merits of the 25-step converter over other structures is that it gives a lower cost, calculated by the CF

$$\mathrm{CF} = \frac{N_{\mathrm{TC}} + \dfrac{\mathrm{TBV}}{V_{\mathrm{o,max}}}}{\mathrm{Gain} \times N_{\mathrm{level}}} \tag{14}$$

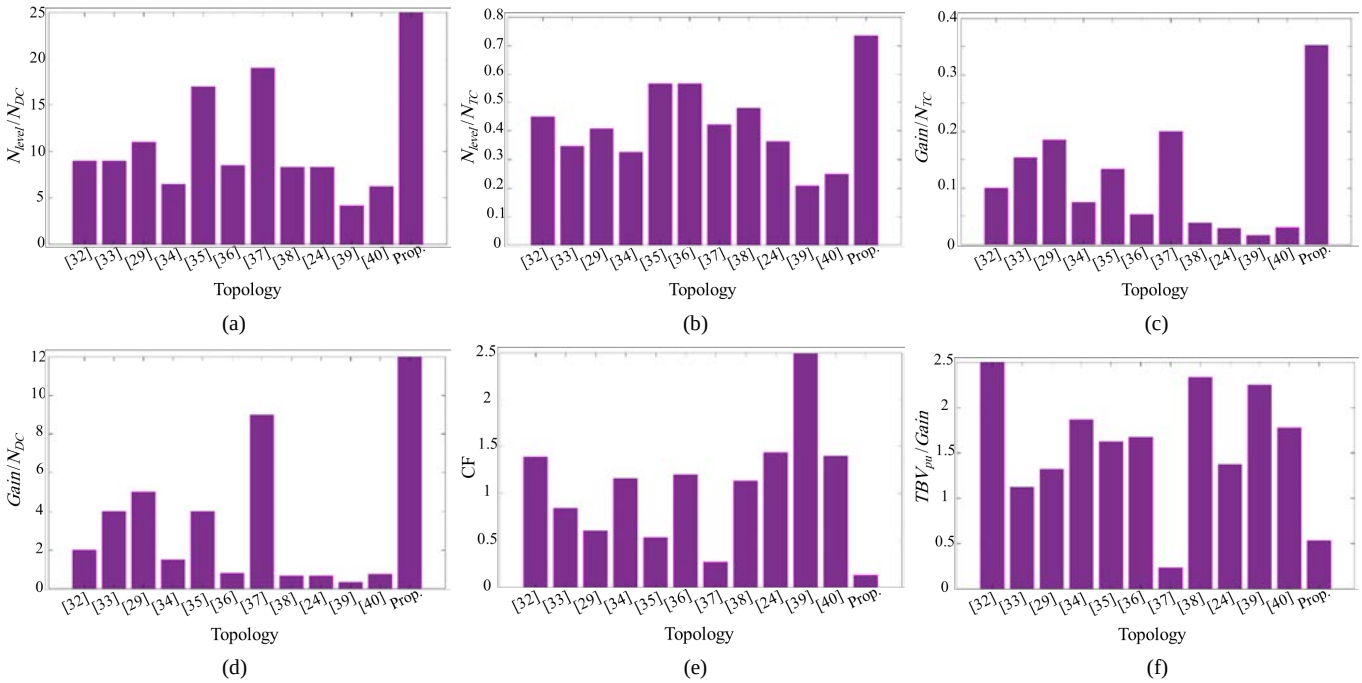


Fig. 5. Comparative results with other topologies. (a) Number of levels per DC source counts. (b) Number of levels per total component counts. (c) Gain per total component counts. (d) Gain per DC source counts. (e) CF. (f) TBV_{pu} per gain. (See also Table IV)

The CF is influenced by the total number of components, the TBV on semiconductors, the number of levels, and the gain, with CF directly related to the first two factors and inversely related to the latter two. Among the topologies, as reported in Table IV, the suggested structure has a lower cost function, as seen in Fig. 5(e). Thus, the suggested configuration can implement 25-step boosted output voltage with fewer switches, capacitors, diodes, and input power supplies, which ensures that the given circuit is both cost-effective and high-performing, making it suitable for practical applications. From Fig. 5(f), it is clear that the TBV_{pu} per gain of the proposed topology is lower than the topologies in [24], [29], [32]-[36], and [38]-[40].

V. Theoretical Analysis and Experimental Results

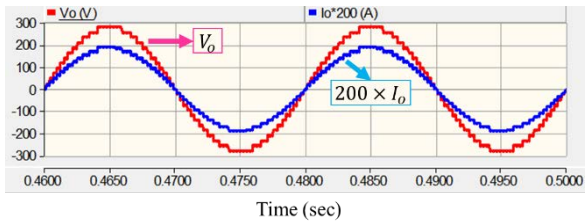
A. Simulation Results

Simulations are executed using PSCAD software, and the parameters are detailed in Table V to assess the performance of the proposed 25-step converter.

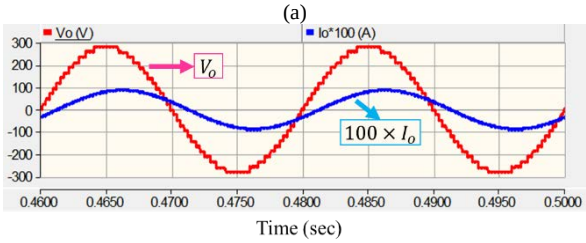
Figs. 6(a) and 6(b) depict the simulated waveforms of the inverter's load voltage (V_o) and current (I_o) for both resistive (R) and resistive-inductive (R-L) loads. Due to the inductive nature of the load, the output current exhibits a smooth waveform. Fig. 6(c) illustrates the harmonic spectrum of the converter output voltage. All high-order harmonics amplitudes are below 1%. Notably, all even harmonics have been effectively eliminated. By analyzing 63 harmonic orders, the THD of the output voltage from the proposed topology is calculated to be 2.23%. However, the THD of the R-L load current waveform is about 0.32%. Consequently, the output filter can either be downsized or eliminated

TABLE V
THE PROPOSED CIRCUIT PARAMETERS IN PSCAD

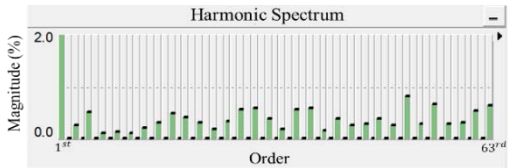
Parameter	Symbol	Value
Input DC source/V	V_{dc}	24
Capacitance of capacitors/μF	C_1-C_4	4700
Output frequency/Hz	f	50
Load	R-L	300 Ω-0.4 H



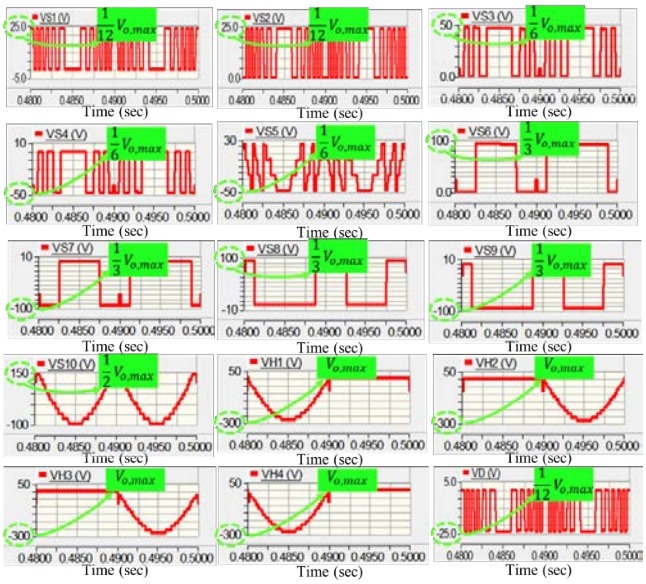
(a)



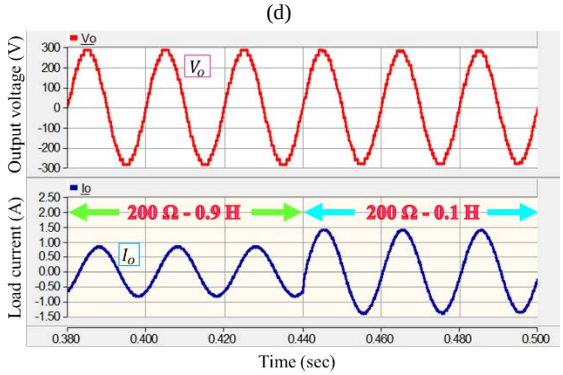
(b)



(c)



(d)



(e)

Fig. 6. Simulated waveforms. (a) Output waveforms for a purely R load. (b) Output waveforms for an R-L load. (c) Output voltage harmonic spectrum. (d) BV on switches and diode. (e) Dynamic performance of resistive-inductive load during inductive changes.

altogether. The BV on semiconductor devices of the proposed topology is shown in Fig. 6(d), which confirms Table II. Fig. 6(e) shows the dynamic performance of the given configuration during inductive load variations. The output voltage remains unchanged, when the inductive load decreases from 0.9 to 0.1 H at 0.44 s. While the load current increases from 0.58 to 1 A (rms: root mean squared). Fig. 7 shows the voltage of capacitors C_1-C_4. The voltages of all 4 capacitors converge to their expected values ($V_{C1} = V_{dc}$, $V_{C2} = 2V_{dc}$, and $V_{C3} = V_{C4} = 4V_{dc}$) with low voltage ripple. This confirms the inherent voltage balancing capability of the proposed topology without the need for auxiliary balancing circuits. The selected capacitance value of 4700 µF ensures stable operation under the applied R-L load. Fig. 8 illustrates the dynamic performance of the proposed inverter under R-L load when the input voltage is varied to emulate photovoltaic voltage fluctuations. At t = 0.3 s, the input voltage increases from 24 to 34 V. As observed, the output voltage scales proportionally with the input voltage, while the load current remains continuous without introducing instability. This confirms the inherent voltage boosting and stable operation of the proposed topology under varying PV input conditions, even in open-loop operation. The output voltage/current waveform for nonlinear load (diode rectifier) is illustrated in Fig. 9(a). The current THD of this scenario is about 1.7%. Additionally, Fig. 9(b) presents the voltage and current waveforms under dynamic conditions for a nonlinear load. At 0.44 s, the inductive component of the nonlinear load increases from 0.1 to 0.4 H, demonstrating the system's response to varying load conditions.

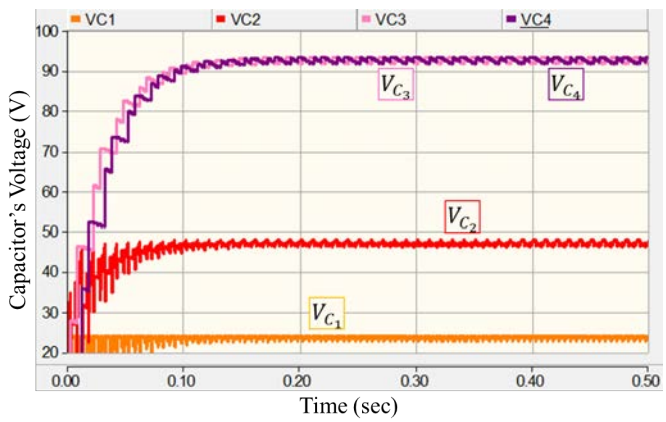


Fig. 7. Simulated voltages of capacitors C_1-C_4 demonstrating stable voltage balancing and low ripple under steady-state operation.

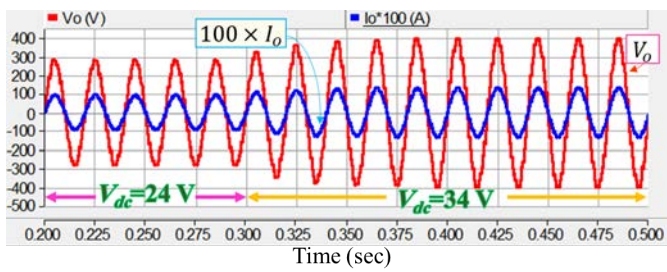
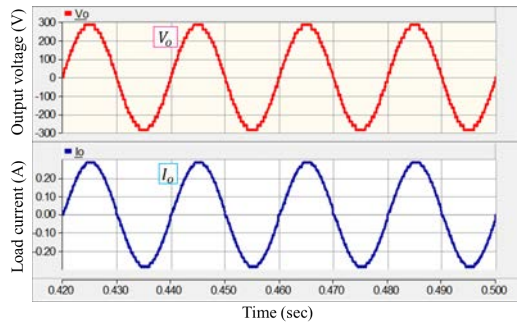
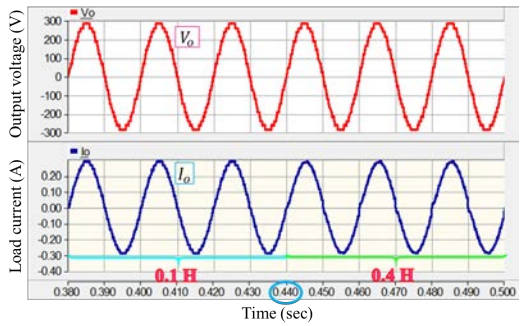


Fig. 8. Dynamic response of the output voltage and load current under RL load when the input voltage is step-changed from 24 to 34 V at t = 0.3 s.



(a)



(b)

Fig. 9. The output voltage and load current for nonlinear load in (a) steady state and (b) dynamic operation (when inductance is changed from 0.1 to 0.4 H at 0.44 s).

The equations of the total loss, losses of switches, capacitors, and diode, as well as the efficiency are determined as:

$$\begin{aligned} P_{\text{loss}}^{\text{total}} &= P_{\text{loss}}^{\text{switch}} + P_{\text{loss}}^{\text{diode}} + P_{\text{loss}}^{\text{capacitor}} \\ P_{\text{loss}}^{\text{switch}} &= \frac{1}{6} f_s V_{\text{stress}} I_{\text{ave}} \left(t_{\text{on}} + t_{\text{off}}\right) + R_{\text{on}} I_{\text{rms}}^2 \\ P_{\text{loss}}^{\text{diode}} &= R_{\text{on}} I_{\text{rms}}^2 + V_{\text{FD}} I_{\text{ave}} \\ P_{\text{loss}}^{\text{capacitor}} &= \frac{1}{2} f_s C \left(\Delta V\right)^2 + \left(R_{\text{ESR}} I_{\text{rms}}^2\right) \\ \eta &= \frac{P_o}{P_o + P_{\text{loss}}^{\text{total}}} \times 100\% \end{aligned} \tag{15}$$

where the fundamental frequency is represented by f_s, while V_{stress} is the voltage stress on a power switch. The rms current and average current are denoted as I_{rms} and I_{ave}, respectively. The on-state resistance of a power switch is symbolized by R_{on}, and the equivalent series resistance is referred to as R_{ESR}. Forward voltage of diode in on-state is symbolized by V_{FD}, and ΔV is the difference voltage of capacitor between maximum value to minimum of it in steady-state. Also, capacitance denotes by C. The turn-on and turn-off time is represented by t_{on} and t_{off}, respectively. Fig. 10 illustrates the 25-level inverter's efficiency versus different values of output power resulting from the simulation. As an example, at an output power of 560 W, the proposed inverter achieves an overall efficiency of approximately 97.2%. To evaluate the degraded-mode operation of the proposed inverter, an open-circuit fault is intentionally introduced in switch S_8. Since S_8 is permanently open under this condition, the original switching table cannot be applied. Therefore, a modified switching strategy is derived by excluding all switching states involving S_8, while preserving valid current paths and capacitor charging sequences. Under this fault condition, the inverter continues operating with 13 output voltage levels and a maximum voltage gain of 6. For an input voltage of V_{dc} = 24 V, the peak output voltage reaches approximately 144 V, as shown in Fig. 11. Although the number of voltage levels is reduced compared to the healthy operation, the inverter maintains continuous power delivery and a stable staircase voltage waveform, validating the FT capability of the proposed topology. To evaluate the closed-loop performance of the proposed multilevel inverter, a voltage control loop based on a proportional-integral (PI) controller is simulated. The controller regulates the peak value of the output voltage by adjusting the modulation reference while maintaining the same DC input voltage. The reference peak output voltage is initially set to 96 V and is reduced to 48 V at t = 0.3 s. As shown in Fig. 12, the inverter output voltage follows the reference accurately with negligible steady-state error, confirming the effectiveness of the closed-loop control strategy. During this transition, the number of voltage levels is automatically reduced from 9 levels to 5 levels, illustrating the inherent adaptability of the nearest-level modulation scheme under closed-loop operation. It is worth noting that, for an input DC voltage of 24 V, the proposed topology is capable of generating a maximum peak output voltage of approximately 288 V with 25 voltage levels under full modulation. The presented closed-loop test case intentionally operates below the maximum gain to demonstrate dynamic voltage regulation, stability, and controllability under varying reference conditions. These results confirm that the proposed inverter is not only suitable for open-loop operation but also exhibits robust closed-loop performance, making it appropriate for practical renewable energy and power conditioning applications.

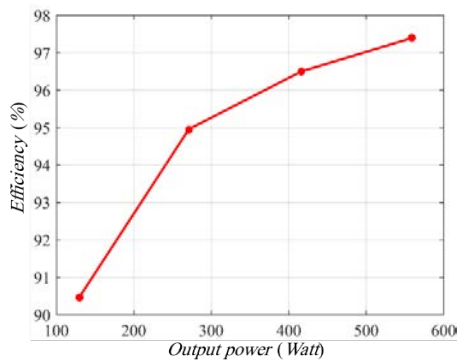


Fig. 10. For constant current, the efficiency of the proposed 25-level inverter versus output power.

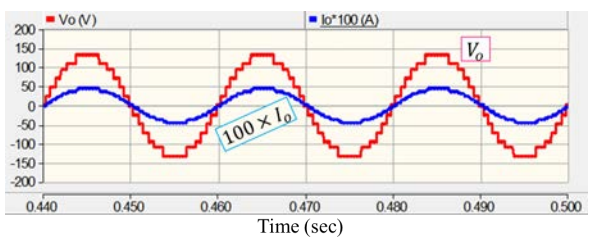


Fig. 11. Output voltage waveform of the proposed inverter under open-circuit fault in switch S_8.

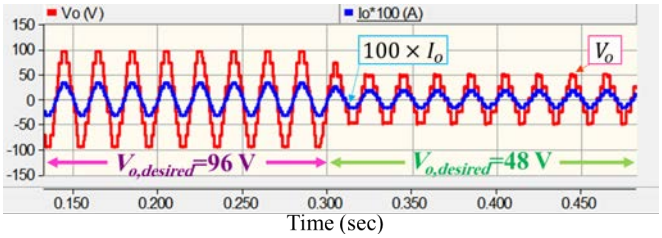


Fig. 12. Closed-loop voltage control performance of the proposed 25-level inverter using a PI controller. The reference peak output voltage is reduced from 96 to 48 V at t = 0.3 s while the input DC voltage is maintained at 24 V.

B. Experimental Results

Fig. 13 shows an experimental setup which has been constructed to validate the practicality of the suggested 25-level inverter circuit and evaluate its performance, in which, the microcontroller atmega32 provides switching pulse of switches S_1-S_{10} and H_1-H_4. To generate ON and OFF pulses for all switches, the microcontroller's output pulses are boosted by a buffer. TLP250 performs the isolation between the control and power sections of the circuit. Eventually, TLPs' output pulse is exerted on the gate bases of each switch. Figs. 14(a) and 14(b) show the inverter's output voltage and current waveforms under R and R-L loads, respectively, in which 20 V input source is applied. Hence, it is observed that the peak voltage is 240 V. This capability to boost the voltage is one of the main advantages of the suggested inverter.

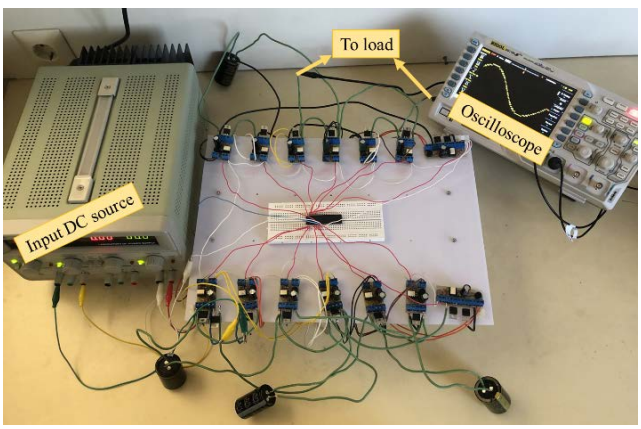
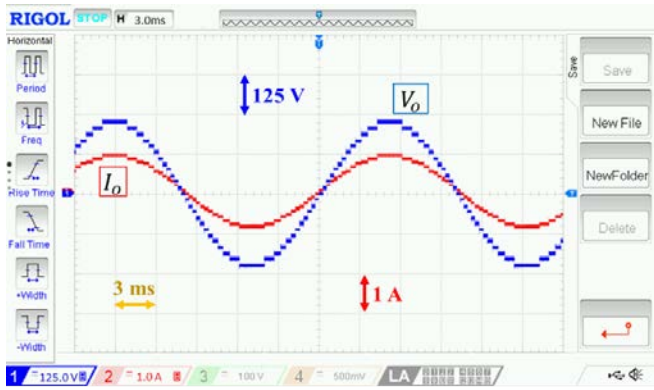


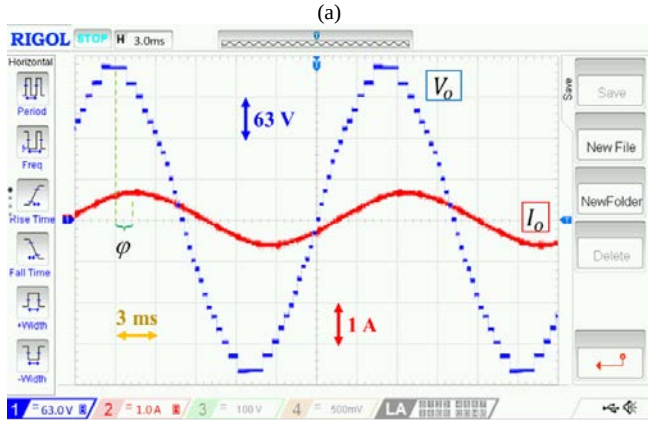
Fig. 13. Experimental setup.

Fig. 15 shows the experimental results of the proposed inverter under dynamic performance. When the load suddenly changes from 300 to 600 Ω, the peak load current decreases from 0.7 to 0.35 A, whereas the changes in load voltage magnitude remain negligible. Under opposite conditions (a sudden load decrease from 600 to 300 Ω), the load peak current is increased twice, but the output voltage amplitude stays almost unchanged. In each scenario, the proposed inverter restores its steady-state operation in less than 0.2 ms, demonstrating the rapid dynamic response of the suggested converter.

Fig. 16 presents the experimental results of the proposed inverter's dynamic performance with a R-L load. When the inductance changes suddenly from 300 Ω, 400 mH to 300 Ω, 600 mH, the peak load current drops from 0.7 to 0.57 A, while



(a)



(b)

Fig. 14. Experimental outcomes of load voltage and current with (a) pure R load (R_L = 300 Ω), (b) R-L load (300 Ω-400 mH).

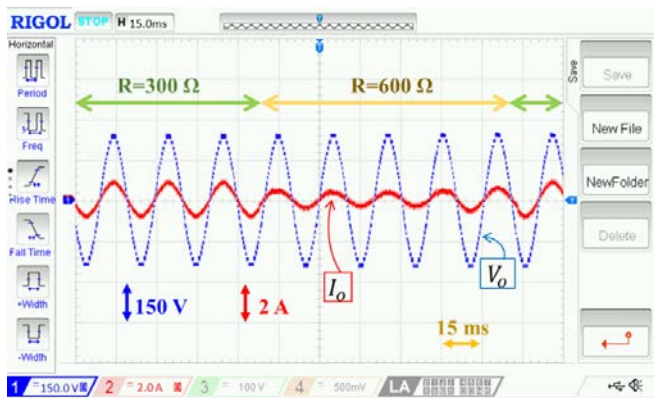


Fig. 15. The suggested topology's dynamic performance.

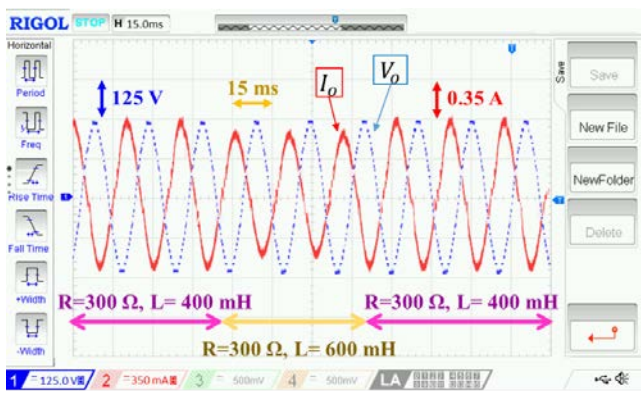


Fig. 16. Proposed inverter's dynamic performance with a resistive-inductive load.

the load voltage variation is ignorable. Conversely, as the inductance shifts back from 600 to 400 mH, the load current increases, while the output voltage amplitude remains stable. It is noteworthy that for ensuring both voltage and current waveforms are clearly visible in the oscilloscope output, the invert key has been applied in this case.

Fig. 17 shows the experimental outcomes of the proposed inverter's dynamic behavior with an R-L load. When the load abruptly shifts from 300 Ω, 400 mH to 600 Ω, 600 mH, the peak load current reduces from 0.7 to 0.37 A. In this scenario, the output voltage amplitude remains on the desired sine waveform, with the voltage and current waveforms adjusted using the invert key.

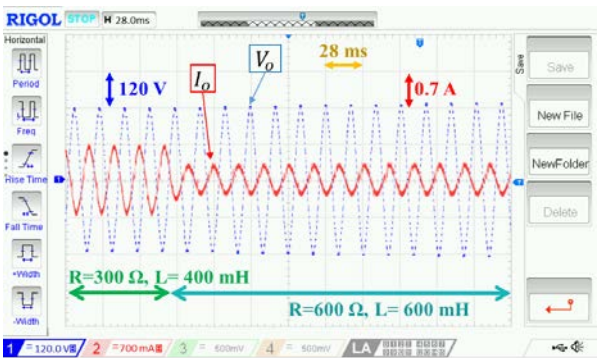


Fig. 17. Dynamic performance of the suggested converter, during both resistive and inductive changes simultaneously.

VI. Conclusion

In this paper, a single-phase 25-step high-gain inverter is suggested for photovoltaic system applications, comprising a combination of an CSM and an HBM. Charging of the capacitors in the given structure occurs in a self-balancing manner, with the charging time being independent of the load. Compared to other step-up multilevel inverters, the proposed structure reduces the number of DC input supplies, diodes, switches, and capacitors, leading to a reduced system volume and cost. The suggested structure offers several key advantages: easy control, simple configuration, precise sine output, and voltage boosting capability. The operational states of the given configuration and its modulation technique, analysis of the capacitors' charging process, and BV of the power switches and diode are comprehensively described. Additionally, a generalized topology composed of cascaded basic modules has been introduced. A comprehensive methodology has been proposed for determining the value of DC supplies in this structure, aiming to reduce redundant switching modes and increase the number of achievable voltage levels. The steady-state and dynamic performances of the proposed 25-level inverter have been validated through simulation and experimental investigations under resistive and resistive-inductive load variations. Furthermore, the efficiency performance of the inverter has been evaluated over a wide output power range based on loss analysis, demonstrating high efficiency and reduced switching losses as a result of the fundamental-frequency nearest-level modulation strategy. The FT capability of the proposed topology has been investigated under open-circuit switch fault conditions, where the inverter continues operating in degraded modes with a reduced number of voltage levels, ensuring continuous power conversion and enhanced operational reliability. Moreover, the closed-loop performance of the proposed inverter has been demonstrated using a PI-based voltage control scheme. The results confirm accurate output voltage tracking, stable transient response under reference voltage variations, and adaptive adjustment of the output voltage levels according to the control command. These features highlight the suitability of the proposed topology for both open-loop and closed-loop controlled applications, making it a promising candidate for practical renewable energy integration and power conversion systems.

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